Docket No.: 204552031600
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
John TWYNAM

Application No.: 10/762,572 Confirmation No.: 3031

Filed: January 23, 2004 Art Unit: 2815

For: COMPOUND SEMICONDUCTOR FET Examiner: E. Lee

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on July 23, 2007, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal
VII.	Argument
VIII.	Claims

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

SHARP KABUSHIKI KAISHA

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 6 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 4
2. Claims withdrawn from consideration but not canceled: none
3. Claims pending: 1-3 and 5-7
4. Claims allowed: none
5. Claims rejected: 1-3 and 5-7

C. Claims On Appeal

The claims on appeal are claims 1-3 and 5-7

IV. STATUS OF AMENDMENTS

Appellant did not file an Amendment After Final Rejection.

Accordingly, the claims enclosed herein as Appendix A incorporate the amendments indicated in the paper filed by Applicant on November 3, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites a compound semiconductor FET (Fig. 1) comprising an undoped AlN layer (element 12, Fig. 1, para. [0023]) provided on a substrate (element 11, Fig. 1, para. [0023]); a plurality of III-N layers (elements 13 and 14, Fig. 1, para. [0023]) provided on the AlN layer, the III-N layers including an undoped GaN layer (element 13, Fig. 1, para. [0023]); an n-type delta doped GaN layer (element 18, Fig. 1, para. [0024]) interposed between the undoped AlN layer (element 12) and the undoped GaN layer (element 13), and having dopant concentration for reducing discontinuity of an electric field at an interface between the undoped AlN layer and the undoped GaN layer (para. [0029]); a source electrode (element 15, Fig. 1, para. [0023]); a gate electrode (element 15, Fig. 1, para. [0023]); and a drain electrode (element 15, Fig. 1, para. [0023]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1 and 2 stand finally rejected under 35 USC 103(a) as being unpatentable over Khan, U.S. Patent No. 5,192,987, in view of Yamashita, U.S. Patent No. 6,995,397 B2.

Claim 3 stands finally rejected under 35 USC 103(a) as being unpatentable over Khan in view of Yamashita as applied to claims 1 and 2, and further in view of Phillips, U.S. Patent No. 6,770,902 B2.

Claims 5 and 6 stand finally rejected under 35 USC 103(a) as being unpatentable over Khan in view of Yamashita as applied to claims 1 and 2, and further in view of Inoue, U.S. Patent No. 6,639,255 B2.

Claim 7 stands finally rejected under 35 USC 103(a) as being unpatentable over Khan in view of Yamashita as applied to claim 1 and 2, and further in view of Abrokwah, U.S. Patent 5,895,929.

VII. ARGUMENT

Claim 1 recites "an n-type delta doped GaN layer ... having dopant concentration for reducing discontinuity of an electric field at an interface between the undoped AIN layer and the undoped GaN layer." The Examiner relied on Yamashita as teaching this feature. However, Yamashita does not teach or suggest selecting the dopant concentration to reduce discontinuity of the electric field at the interface the AlN layer and the undoped GaN layer. Although Yamashita contains a discussion relating to the dopant concentration of the delta doped layer 21, the dopant concentration in Yamashita's structure is not selected to reduce discontinuity of the electric field at the interface the AlN layer and the undoped GaN layer. Specifically, the weakened electric field in the surface region of the channel layer 20 in Yamashita's structure results not from reduction of discontinuity of the electric field, but from the "pinch off point" maintained at the deeper portion of the channel layer 20 away from the surface thereof.

In other words, the claimed dopant concentration is selected so as to reduce discontinuity of the electric field of the interface, whereas the dopant concentration in Yamashita's structure is not intended for such reduction of electric field discontinuity.

In the Advisory Action dated July 31, 2007, the Examiner stated the claim recitation "an n-type delta doped GaN layer . . . having dopant concentration for reducing discontinuity of an electric field at an interface between the undoped AIN layer and the undoped GaN layer" is merely a limitation directed to the manner in which the apparatus is intended to be employed and therefore does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations (citing *Ex Parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987)). Appellant respectfully disagrees.

The claim limitation "an n-type delta doped GaN layer . . . having dopant concentration for reducing discontinuity of an electric field at an interface between the undoped AIN layer and the undoped GaN layer" clearly defines the structure itself and does not relate to the manner in which the apparatus is intended to be employed. Claim 1 recites a compound semiconductor FET, which is made up of the layers shown in Fig. 1 and recited in claim 1. The n-type delta doped layer is obviously doped, and the dopant concentration must be selected to some value for the actual construction of the FET. The above-quoted limitation merely sets that dopant concentration and does not relate to a manner in which the FET is used. This limitation clearly limits the structure itself, and thus should be afforded patentable weight. As such, since Yamashita does not teach or suggest selecting the dopant concentration to reduce discontinuity of the electric field at the interface the AlN layer and the undoped GaN layer, this rejection should be reversed.

The remaining claims are allowable at least due to their dependency from claim 1. Appellant requests that the remaining rejections be reversed.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A do include the amendments filed by Applicant on November 3, 2006, and do not include the amendment(s) filed on September 7, 2007.

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Dated: September 19, 2007

Respectfully submitted,

By 

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/762,572

1. A compound semiconductor FET comprising:

an undoped AlN layer provided on a substrate;

a plurality of III-N layers provided on the AlN layer, the III-N layers including an undoped GaN layer;

an n-type delta doped GaN layer interposed between the undoped AlN layer and the undoped GaN layer, and having dopant concentration for reducing discontinuity of an electric field at an interface between the undoped AlN layer and the undoped GaN layer;

a source electrode;

a gate electrode; and

a drain electrode.

2. The compound semiconductor FET according to claim 1,

wherein the plurality of III-N layers comprise an AlGaN layer formed on the undoped GaN layer, and

wherein the source electrode, the gate electrode, and the drain electrode are provided on the AlGaN layer.

3. The compound semiconductor FET according to claim 1, further comprising an insulating layer on an uppermost layer of the plurality of III-N layers,

wherein the plurality of III-N layers comprise an AlGaN layer formed on the undoped GaN layer,

wherein the source electrode and the drain electrode are provided on the AlGaN layer, and

wherein the gate electrode is provided on the insulating layer.

5. The compound semiconductor FET according to Claim 1, wherein material of the substrate is sapphire,

wherein each of the semiconductor layers formed upon the substrate is of a C-plane Ga-surface type, and

wherein sheet doping concentration of the n-type delta doped GaN layer is within a range of 1×10^{13} cm^{-2} to 2×10^{13} cm^{-2}.

6. The compound semiconductor FET according to Claim 1, wherein material of the substrate is SiC,

wherein each of the semiconductor layers formed upon the substrate is of a C-plane Ga-surface type, and

wherein sheet doping concentration of the n-type delta doped GaN layer is within a range of 5×10^{12} cm^{-2} to 1.5×10^{13} cm^{-2}.

7. An electronic circuit provided with the compound semiconductor FET as defined in claim 1.